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DETERMINING PROCESS LATITUDE WITH ELECTRICALLY MEASURABLE TEST STRUCTURES

by

Jonathan A. Littlehale

A Thesis Submitted

in

Partial Fulfillment

of the

Requirements for the Degree of

MASTER OF SCIENCE

in

Electrical Engineering

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DEPARTMENT OF ELECTRICAL ENGINEERING

COLLEGE OF ENGINEERING

ROCHESTER INSTITUTE OF TECHNOLOGY

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PREFACE

The work described herein has served a dual purpose: first as partial fulfillment of the requirements for the Degree of Master of Science in Electrical Engineering from Rochester Institute of Technology, and second as an integral part of my work assignment in the Device Technology Lab of the Kodak Research Laboratories. This arrangement has permitted extensive use of state-of-the-art VLSI design, processing, and testing equipment as well as access to useful statistical analysis software.

This work was made possible through the generous support of Dr. Thomas M. Kelly and with guidance and assistance from Dr. Robert E. Cookingham, Dr. Edward T. Nelson (reticle design and layout), and Mr. John R. Fischer and Mr. Dennis J. Lorei (device testing), all of Eastman Kodak Company.

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by

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ABSTRACT

Collection of linewidth data is an important part of photoresist characterization. Linewidth data are usually collected by optical measurements or scanning electron microscopy. Both of these techniques are tedious and time-consuming. In this work, electrically measurable test structures are used to collect linewidth data. These structures use a measured sheet resistance, a known length of conducting material, and the measured resistance of the structure to determine the linewidth. The benefits of using these structures include completely automated data collection and the ability to collect statistically significant amounts of data. This allows the use of existing statistical analysis software to analyze and fit a model to the data. In this study, electrically testable linewidth structures are used in two photoresist characterization experiments to provide important process latitude information. The measured linewidth includes the effects of the photolithography and the subsequent etching step.

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I. INTRODUCTION

The fabrication process for integrated circuits involves a number of repetitions of the following series of steps: cleaning, material deposition, patterning, and etching. Patterning is achieved through a photolithographic process. The patterning process (simplified) is as follows: coat photoresist, prebake, expose, develop photoresist, postbake.

The patterned photoresist selectively protects a previously deposited material from the subsequent etching step. After etching, since the desired pattern has been transferred to the underlying material, the remaining photoresist is removed and the cycle repeats, beginning with cleaning and material deposition.

The objective of the patterning process is to accurately and repeatably reproduce given patterns which will each become a layer of an integrated circuit. Failure to provide faithful reproduction of the desired pattern can cause complete device failure. To attain the accuracy and repeatability required for success, an in-depth understanding of the photolithographic process is essential.

Photoresist characterization is a time-consuming and often tedious chore that provides the processing engineer with important operating point information as well as some understanding of the results of small process variations around that point. The list of variables to be investigated is long: prebake time, prebake temperature, exposure time, developer concentration, developer temperature, development time, postbake time, postbake temperature. The relationships between these variables and linewidth, remaining resist thickness, and resist profile are desired. The complexity of full resist characterization experiments is staggering. Most experiments require much process time and very many data to be collected, compressed, and analyzed.

A method for reducing the difficulty of photoresist characterizations will be discussed. This method involves the collection of linewidth data, often considered the bottom line of any resist characterization. These data may be collected in a number of ways: optical scanning and reflection analysis, scanning electron microscopy, and electrically testable linewidth structures. Of these, the first two techniques are often used because they measure the width of the line in a "direct" manner. Unfortunately, these techniques are subject to errors caused by resist profile, equipment calibration, and other measurement difficulties. In addition, much time is required to collect the data. The third technique, electrically testable linewidth structures, represents a measurement that is not "direct" but relative, since the electrical linewidth is measured and may not be identical to the physical width. The measured linewidth is the result of the entire patterning process, i.e., the photolithography and the subsequent etch step. However, this method can be automated. Automation provides rapid data collection and compression. The results obtained will provide the relationships between the variables under investigation.

An additional method for reducing the difficulty of photoresist characterizations is statistical experiment design. This method can be used to reduce the number of data points required to determine processing relationships without losing the accuracy of larger experiments. In this work, electrically testable linewidth structures and statistical experiment design were used to characterize photoresist processing on doped polysilicon.

II. REVIEW OF LITERATURE

Truly complete resist characterization includes not only monitoring the results of the photolithographic process but also monitoring the response of the photoresist to each individual step of the process. Much work has been done to investigate photoresist. K. G. Clark[1] presents an overview of both positive and negative photoresists and the associated chemistry. He also shows the relationship between resist thickness and spin speed. Also investigated are spectral sensitivity of resist and the affect of prebake on resist performance. Similarly, Hryhorenko[2] investigated the relationship between linewidth and exposure, resist thickness, development time, developer temperature, developer concentration, postbake time, and postbake temperature. He also discusses equipment calibration and process optimization. An in-depth study of resist thickness and the parameters that influence it is given by Meyerhofer.[3]

In order to increase the understanding of photoresist processing, various modeling programs have been developed. One such program is called SAMPLE.[4] SAMPLE is able to model photolithographic processing as well as various etching processes. After input of initial conditions and desired processing conditions, SAMPLE performs the required calculations to arrive at a predicted edge profile. The calculated edge profile can be compared to SEM's of processed resist to verify the predicted resist loss during development and compare the predicted standing wave patterns to those actually obtained. The model can be made to fit the experimental results by varying the parameters A, B, and C. Methods for determining A, B, and C independently have been developed.[5-7] Although SAMPLE is the most well known and is readily available, other resist models have been developed.[8-10]

Positive photoresist development has evolved from batch submersion to in-line spray development[11] to in-line puddle development. Puddle development combines the convenience of single wafer processing with the consistency of submersion.[12] Often, the optimum development process depends on the particular resist being used and the results desired.

Resist technology itself has evolved from negative resist[13,14] to positive resist, which provides higher resolution. The increasing demand for higher density integrated circuits has pushed resolution requirements to the 2.0 to 3.0 μm level for production processes, the 1.0 to 2.0 μm level for development work, and into the submicron region for state-of-the-art research processes. Because of the theoretical limits of optical resist exposure techniques,[15] new methods of exposure are being investigated.

Some of these lithography methods are electron beam, x-ray, ion beam, and laser.[16] A comparison of optical and electrical beam lithography for 1 μm geometries is presented by Chang et al.[17] M. W. Levi discusses the production use limitations of the newer single beam lithography techniques.[18]

Smaller geometries are becoming part of the "standard" process. Along with the new processing techniques and equipment required to produce fine geometries is the need for greater process control. A number of studies have been done that describe the sources of linewidth variation and attempt to quantify the contribution of each to the total. Several authors have discussed linewidth control problems due to steps in the underlying topography, interference effects, layer thicknesses, substrate reflectivity, illumination uniformity, exposure time, and focus.[19,24] Some of the problems encountered in measuring linewidths are discussed by Bosenberg[25] (reflection, equipment calibration, line profile.) In addition to control of linewidth, control of the exposure equipment parameters, such as registration and magnification, must be monitored closely.[26-28]

Each of the investigations discussed above requires the collection of substantial amounts of data. Some of the equipment used for collection of various types of data is listed here: ellipsometer, four-point probe, scanning electron microscope, optical microscope, verniers (fabricated with the device), and various electrical test structures.

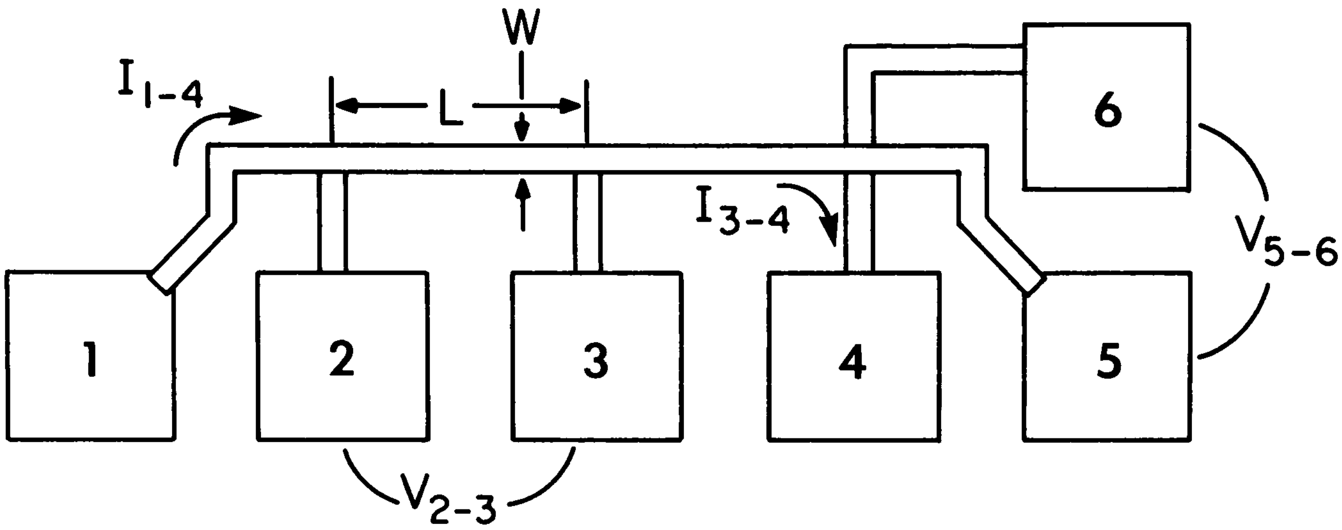
The first report on the use of an electrical test structure was written by L. J. van der Pauw in 1958.[29] His work contains a method for measuring the sheet resistance of a flat sample of arbitrary shape. Four probes are placed in contact with the sample to be measured. A current is forced between two of the probes and the voltage across the other two is measured. This technique has come to be known as the four-point probe method. D. S. Perloff later (1977) presented correction factors for four-point sheet resistance measurements of thin rectangular samples.[30] He concluded that square probe arrays are least error prone, provided the probes are located at the midpoint of the sides. In the same year, David and Buehler published an analysis of various cross sheet resistor test structures, including the effects of arm width and length.[31] Buehler subsequently published several papers concerning the use of electrical test structures for characterizing the linewidth of conducting layers.[32,33] Electrical test structures have also been devised for the measurement of registration errors[34] and monitoring exposure equipment performance.[35]

In general, photoresist characterization has not taken advantage of electrical test structures, even though these test structures depend on photoresist processing. It seems appropriate, then, to apply electrical test structures to photoresist processing and investigate the data that are obtained.

III. RETICLE DESIGN

This study made use of an electrical linewidth structure that is commonly used in the I.C. industry. It consists of a van der Pauw sheet resistance structure and a linewidth measurement structure (Figure 1). Pads 3-6 are used to make the sheet resistance measurement, and pads 1-4 are used for the linewidth measurement. The linewidth measurement is made by forcing a current between pads 1 and 4 and measuring the voltage between pads 2 and 3. This yields the resistance between pads 2 and 3. Since the resistance is equal to the sheet resistivity times the length of the structure divided by its width and three of the four components are known, the width of the line can be calculated. This value of linewidth is the electrical linewidth and is probably not identical to the optical or patterned linewidth. This situation is acceptable when one is looking for relative changes in linewidth that result from process changes.

The objective of this study was to demonstrate the effectiveness of using electrically measurable test structures to characterize photoresist processing. This can be done with just one of the structures described above. The reticle for this study was designed to allow for many other related experiments as well.



$$R_S = \left(\frac{\pi}{\ln 2}\right)\left(\frac{V_{5-6}}{I_{3-4}}\right)$$

$$W = R_S L \left(\frac{I_{1-4}}{V_{2-3}}\right)$$

Figure 1: Electrical linewidth test structure and equations for sheet resistance R_S and linewidth W.

The reticle design contains electrically measurable linewidth test structures oriented in both the x and y directions with linewidths of 0.8, 1.0, 1.2, 1.6, 2.0, 4.0, 8.0, and 12.0 um; large van der Pauw structures for cross checking sheet resistance; evenly spaced and double-spaced lines and spaces of 0.8, 1.0, 1.2, 1.6, 2.0, and 4.0 μm for examination of resist or line profiles and proximity effects; and resolution charts for visual estimation of the smallest geometry defined and the relative exposure. The linewidth structures are combined into groups of two inside a 12-pad structure to allow for ease of testing. (The 12-pad pattern was already in use at Kodak.) Figure 2 shows the 12-pad structure containing the 1.0 and 2.0 μm linewidth test structures. Three similar 12-pad structures contain the 1.2 and 1.6 μm lines, the 0.8 and 4.0 μm lines, and the 8.0 and 12.0 μm lines. An additional 12-pad structure contains two large van der Pauw patterns. These five 12-pad structures were arranged somewhat symmetrically in a cell, which was repeated nine times to form the whole die pattern. The cell also contained long line and space structures with equal lines and spaces and with double-spaced lines. Two resolution charts were also included. Figure 3 shows the cell alone, and Figure 4 shows the whole die pattern.

Repetition of the test structures in the x and y directions provides a means for checking stage stability

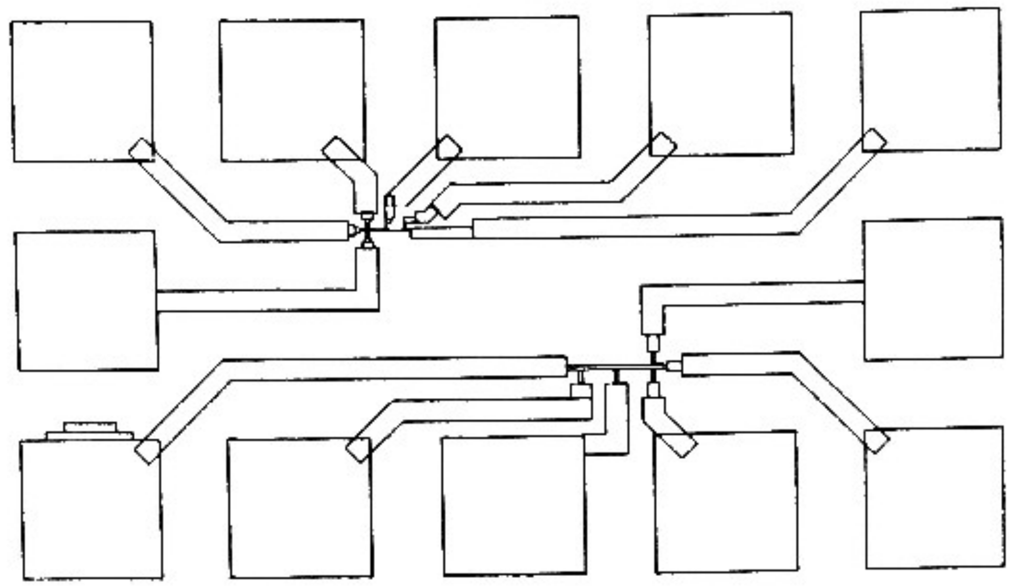


Figure 2: Twelve-pad structure containing 2.0 and 1.0 μm lines.

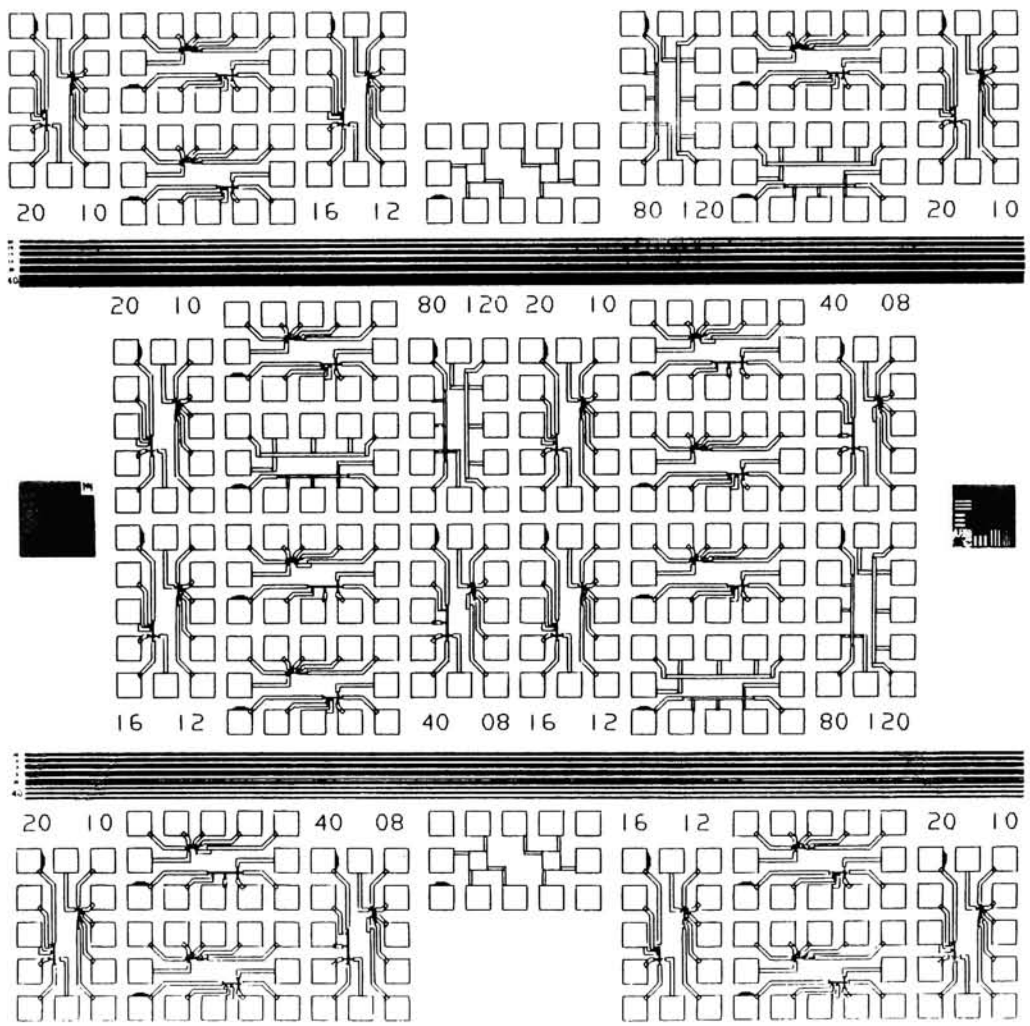


Figure 3: Cell containing linewidth test structures, resolution charts, long lines, and van der Pauw structures.

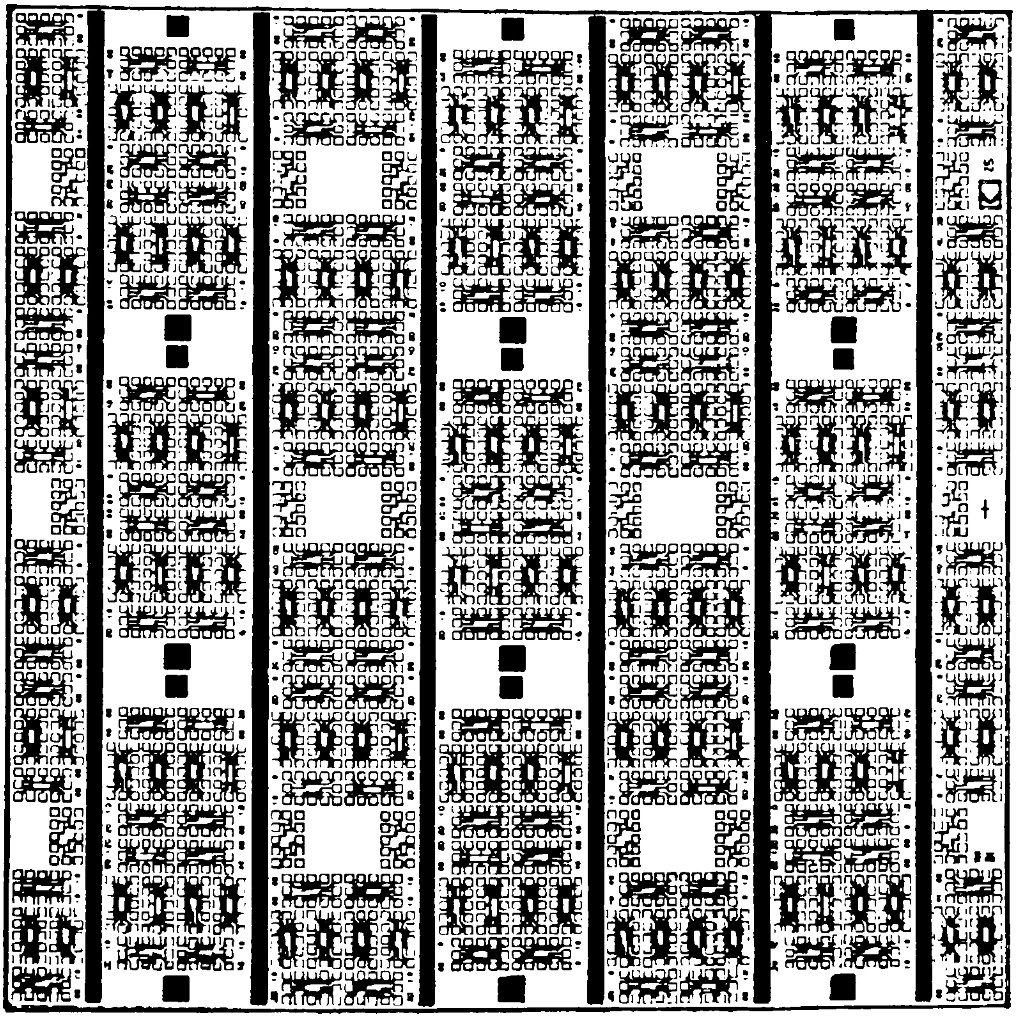


Figure 4: Full die pattern.

(small vibrations in either drive motor during exposure will cause linewidth variations). Since a single die fills the entire exposure field of the stepper, repetition of the linewidth test structures at the edges and throughout the field will allow for illumination uniformity studies. In addition, the reticle was produced (by using e-beam) in both negative and positive tones so that diffused areas (spaces) and patterned materials (lines) could be investigated.

IV. EXPERIMENTAL DESIGN

Large and complicated experiments are not required to demonstrate the concepts proposed in this study. Typical photoresist characterization studies can include as many as seven or more variables. The most often monitored results are critical dimension (linewidth), thickness after development, and resist profile. Two experiments were chosen to verify and demonstrate the use of electrically testable linewidth structures. The first experiment has two variables. In this experiment development time and exposure time were varied while all other process parameters were held constant. The monitored result is linewidth.

A reasonable size for the first experiment is five values for each variable. If all of the 25 possible combinations of variable values are used, the experiment is called "full factorial". This type of experiment is large with two variables but would become immense with three or more variables. A method for reducing the size of experiments is statistical experimental design and is available in an in-house software package called DESRA (Design, Evaluation, Storage, Retrieval, Analysis). DESRA makes use of the commercially available Statistical Analysis System (SAS).[36] DESRA allows for full factorial experiments as well as composite design experiments that cover the same experimental space as the full factorial but greatly reduce the required number of data points. This reduction is achieved by choosing statistically significant variable combinations that will provide the most information about the relationships between variables. The reliability of a composite design can be enhanced by repeating the most important variable combinations, i.e., the center point and the most extreme variable values. DESRA facilitates this option. This package also randomizes the order of the experimental conditions and provides a worksheet to follow as the experiment is carried out. Randomization helps to reduce the effects of systematic errors introduced by the equipment, the experimenter, or processing. DESRA was used to provide both full factorial and composite designs for the experiment in this study. The work sheets for this experiment are shown in Figures 5 and 6.

In considering the experiment to be performed, care must be taken to ensure that the extreme values of the variables will provide useful data, because DESRA requires these data for modeling the variable relationships. It is a good idea to do a quick experiment to delineate the perimeter of the useful experimental space. For example, a short exposure and a short development time may produce areas of residual resist that will result in insufficient etching and shorting of the test structure. For this study it was

DEVELOPMENT TIME vs. EXPOSURE
POLYSILICON LINES

Reference Number	Development (Sec)	Exposure Time (Sec)
11	32	260
25	52	360
3	42	160
1	32	160
13	42	260
20	52	310
22	37	360
16	32	310
5	52	160
9	47	210
10	52	210
19	47	310
18	42	310
4	47	160
14	47	260
7	37	210
6	32	210
21	32	360
2	37	160
12	37	260
15	52	260
8	42	210
24	47	360
23	42	360
17	37	310

Figure 5: Randomized worksheet for full factorial design.

DEVELOPMENT TIME vs. EXPOSURE (COMPOSITE DESIGN) POLYSILICON LINES

Reference Number	Development (Sec)	Exposure Time (Sec)
8	42	360
5	32	260
6	52	260
2	47	210
1	37	210
7	42	160
9	42	260
3	37	310
4	47	310

Figure 6: Randomized worksheet for composite design experiment.

determined that at a development time of 32 sec, the lowest exposure time allowable was 160 msec. The values selected for development time were 32, 37, 42, 47, and 52 sec. The values selected for exposure were 160, 210, 260, 310, and 360 msec.

Once the experiment is finished, the data are entered into the computer and DESRA is used to model the interactions between variables. The data from the full factorial experiment will result in one set of coefficients for the variables and the data from the composite design experiment will result in a second set of coefficients. By performing the full factorial experiment and using the data obtained to derive both models, the accuracy and the value of the shortened experiment can be observed. In general, when the composite design is the only experiment to be done, critical operating points will be repeated in order to improve the reliability of the resulting model.

The variables for the second experiment were exposure time, development time and developer concentration. In planning this experiment, five levels of developer concentration were selected: 40%, 45%, 50%, 55%, and 60%. The same development times and exposures as used in the first experiment were to be used in this experiment. An initial screening experiment was performed and it was found that combinations of the extreme values of the three variables produced either total loss of the two micron line or incomplete development of the surrounding photoresist. In order to obtain measurable results, only the three center values for each variable were used for this second experiment.

V. PROCESSING

The processing required for this study is minimal. The wafers are initially cleaned, and 1000 Å of thermal oxide is grown. A 4000 Å layer of polysilicon is deposited and subsequently doped with phosphorus. The wafers are coated with photoresist and prebaked and are then ready for exposure. (See Appendix for more information.) The dark-field version of the reticle is used to pattern lines on the wafers. Each wafer has 52 dies but represents one experimental condition, e.g., an exposure of 200 msec and a development time of 30 sec. After development and postbake, the pattern is plasma etched into the polysilicon and the photoresist is plasma stripped. The wafers are then ready for testing.

The linewidth structures were tested on a computer-controlled automatic probing station. For the first experiment, twenty-five of the 52 dies were tested. For the second experiment, thirty-six of the dies were tested. An average and a standard deviation were automatically calculated for each wafer. The program first measures the sheet resistance of the van der Pauw structure, measures the voltage drop over a ten-square resistor while forcing a given current, and then calculates the change in linewidth relative to the designed value. A typical printout of resistivity and linewidth change is shown in Figure 7. The time required to test each wafer is less than 3 min.

Patterning of polysilicon lines was chosen for this study because of ease in testing: ohmic contacts are formed between the probes and the doped polysilicon, and the resistivity of the material is reasonable - about 25 ohms/square or 250 ohms for a ten-square resistor. There are, however, several potential difficulties that might result in errors or inability to measure the test structures. Since the polysilicon must be etched to define the test structures, the etching step directly affects measured results. Inconsistencies in the etch, within a wafer or wafer to wafer, will produce variability in the results. In a single-wafer plasma etcher, as used in this experiment, the etching proceeds from the edge of the wafer to the center and will tend to produce edge-to-center variations in the measured linewidth. Also, heating of the etching chamber during the etching of a series of wafers can cause wafer-to-wafer variations in the etch until an equilibrium temperature is reached. Maintaining the randomization of the wafers should reduce this affect. In addition, during the etch it is possible to undercut a narrow resist line and leave a broken polysilicon line, or etch the polysilicon away completely. This must be considered when choosing the extreme values for the variables.

```
21;20   RHO =   19.44   DEL-W = -.80
21;21   RHO =   20.85   DEL-W = -.67
21;22   RHO =   21.67   DEL-W = -.52
21;23   RHO =   22.20   DEL-W = -.54
21;24   RHO =   20.91   DEL-W = -.84
22;24   RHO =   20.15   DEL-W = -.64
22;23   RHO =   21.96   DEL-W = -.58
22;22   RHO =   22.52   DEL-W = -.57
22;21   RHO =   23.31   DEL-W = -.58
22;20   RHO =   21.99   DEL-W = -.67
23;20   RHO =   20.53   DEL-W = -.70
23;21   RHO =   22.75   DEL-W = -.60
23;22   RHO =   21.92   DEL-W = -.65
23;23   RHO =   20.22   DEL-W = -.63
23;24   RHO =   19.16   DEL-W = -.67
24;24   RHO =   20.28   DEL-W = -.62
24;23   RHO =   20.14   DEL-W = -.66
24;22   RHO =   23.81   DEL-W = -.54
24;21   RHO =   24.53   DEL-W = -.57
24;20   RHO =   20.59   DEL-W = -.71
25;20   RHO =   22.31   DEL-W = -.63
25;21   RHO =   20.24   DEL-W = -.77
25;22   RHO =   20.40   DEL-W = -.68
25;23   RHO =   19.96   DEL-W = -.69
25;24   RHO =   20.19   DEL-W = -.64

RHO-AVG  21.28   S.D. 1.399   NO. PTS  25
W-AVG     -.65   S.D. .0796   NO. PTS  25
```

Figure 7: Typical testing output.

VI. RESULTS AND ANALYSIS

The results of the development time vs. exposure experiment are shown in Table 1. Each entry is the average linewidth for the single wafer processed at the corresponding conditions. These data are shown graphically in Figures 8 and 9. In general, these graphs illustrate the expected relationships between development time and delta linewidth and between exposure time and delta linewidth. As exposure time is increased, delta linewidth increases, i.e., the resulting linewidth decreases. Similarly, as development time is increased, delta linewidth increases. This is reasonable because longer exposure times will cause more resist to be exposed by scattered light and be developed away, and longer development times will allow the developer to continue to attack the unexposed resist once the exposed resist is dissolved.

Table 1: Delta linewidth (μm) for development time vs. exposure experiment

Exposure	Development Time (sec)				
(msec)	32	37	42	47	52
160	+0.17	-0.13	-0.28	-0.40	-0.44
210	-0.40	-0.52	-0.57	-0.67	-0.72
260	-0.63	-0.64	-0.78	-0.80	-0.81
310	-0.78	-0.86	-0.80	-0.88	-0.89
360	-0.85	-0.88	-0.93	-0.95	-0.96

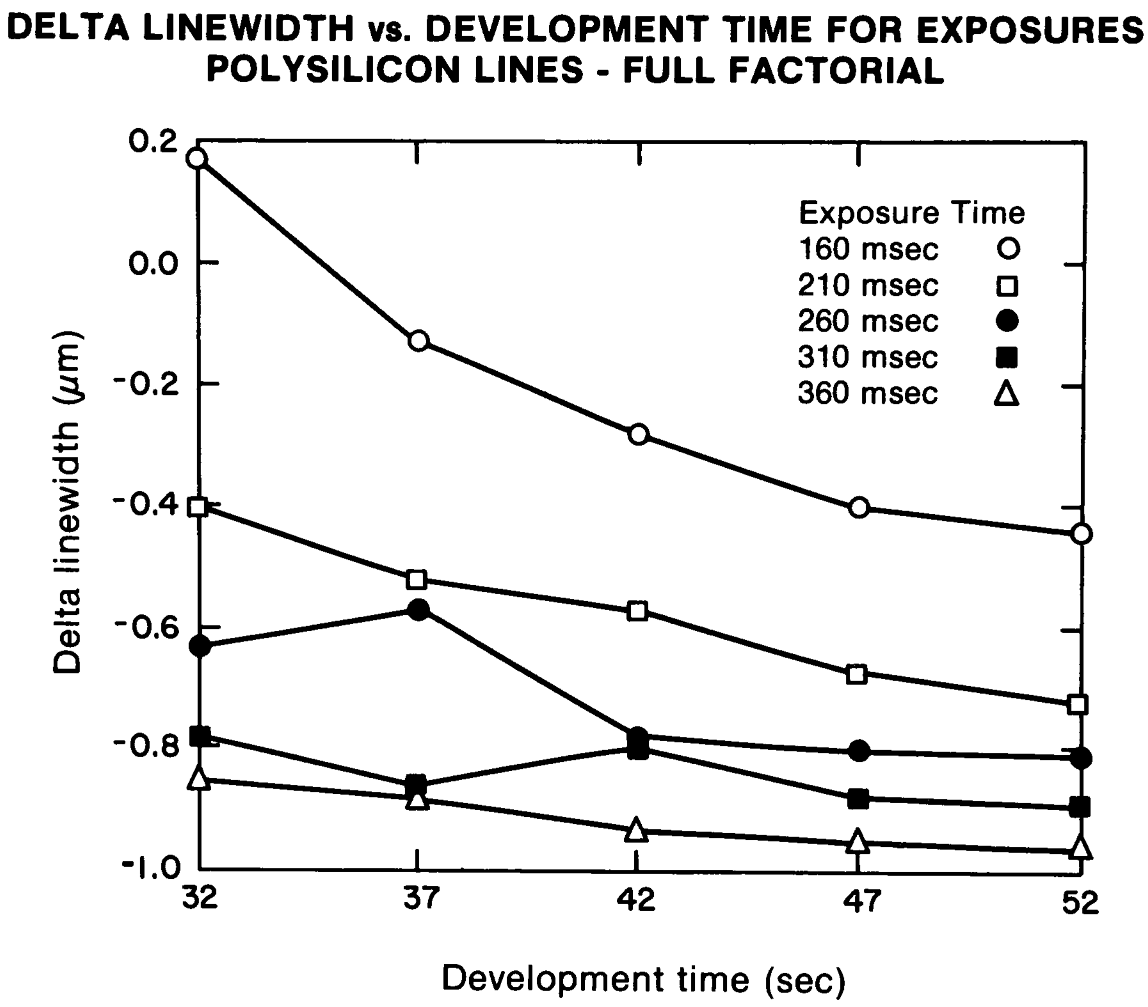


Figure 8: Delta linewidth vs development time, raw data.

DELTA LINEWIDTH vs. EXPOSURE FOR DEVELOPMENT TIMES POLYSILICON LINES - FULL FACTORIAL

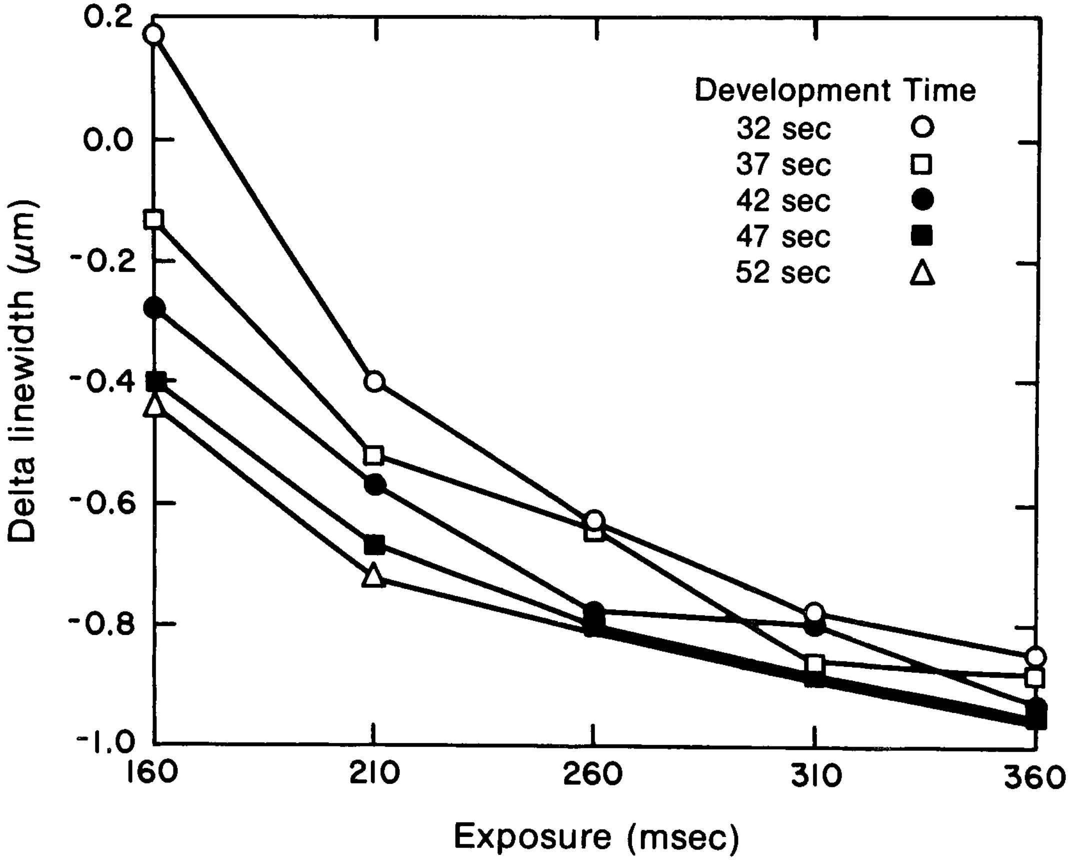


Figure 9: Delta linewidth vs exposure time, raw data.

DESRA was used to create a model for the data obtained in the development time vs. exposure experiment. The model is a linear equation for delta linewidth in terms of development time, exposure time, development time squared, exposure time squared, and development time times exposure time. Higher order terms were included in the model, but their coefficients are not presented here. Table 2 shows the coefficients obtained for the full factorial experiment and for the composite design experiment. The coefficients are not directly related to the relative influence of a variable on delta linewidth. The models are plotted against the data in Figures 10 and 11; correlation is good.

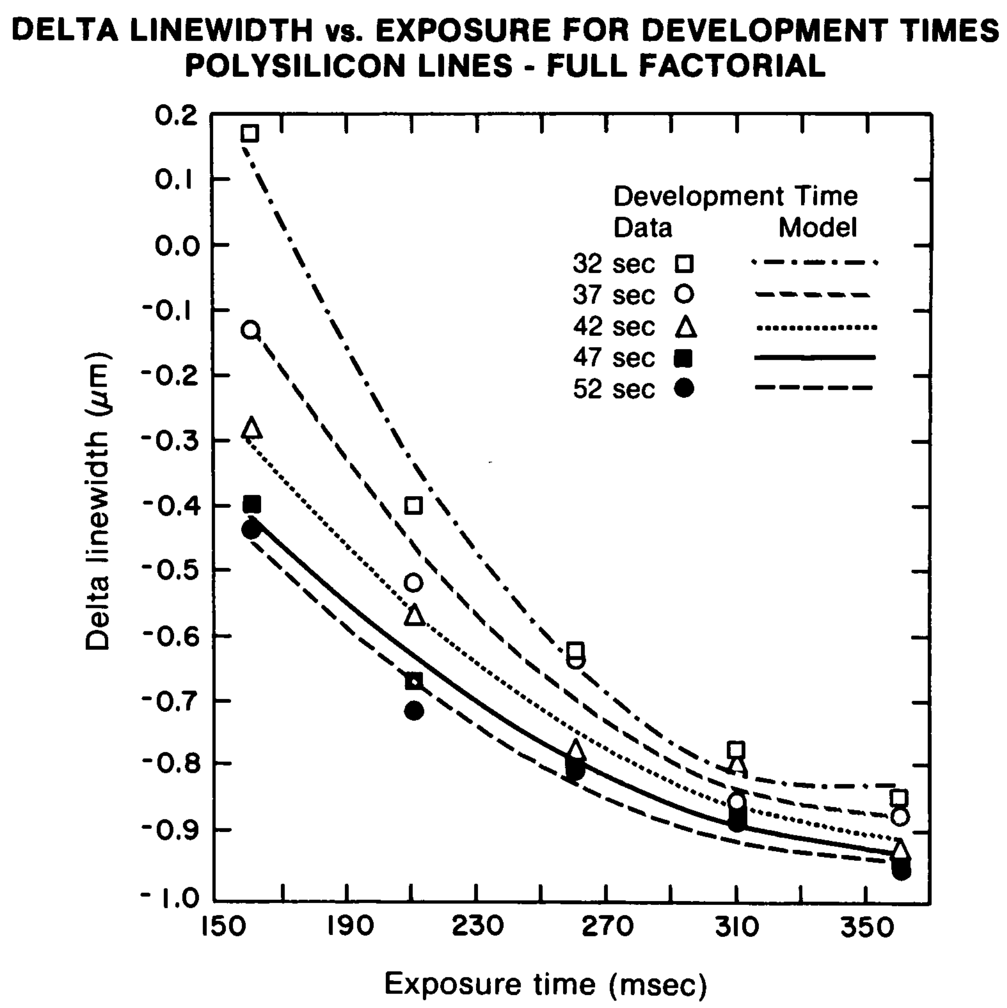


Figure 10: Model and data for delta linewidth vs exposure time, full factorial experiment.

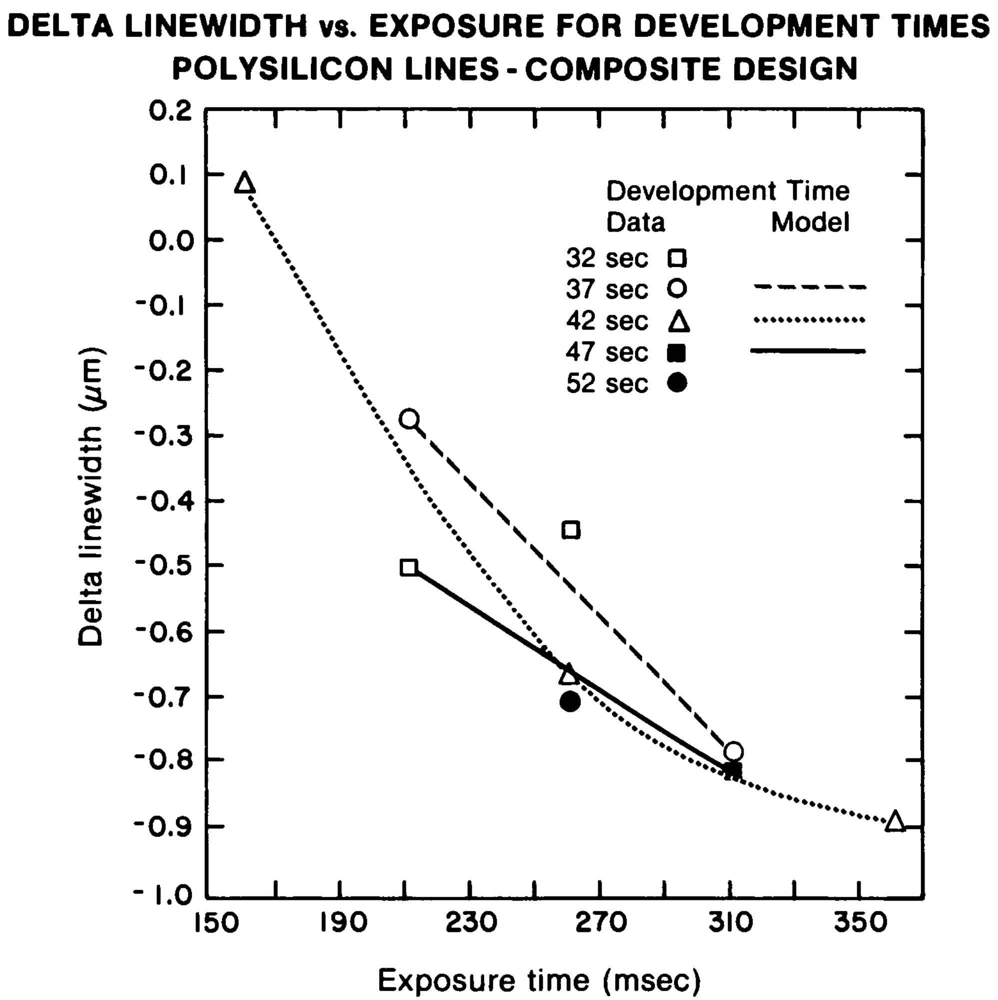


Figure 11: Model and data for delta linewidth vs exposure time, composite design experiment.

Table 2: Model coefficients for full factorial and composite design experiments

Term	Coefficient	
	Full Factorial	Composite
Intercept	-0.75	-0.78
Development Time	-9.063×10^{-3}	-9.000×10^{-3}
Exposure	-3.024×10^{-3}	-3.250×10^{-3}
$(\text{Dev. Time})^2$	1.027×10^{-4}	6.000×10^{-4}
(Dev. Time) x (Exp)	1.180×10^{-4}	1.300×10^{-4}
$(\text{Exposure})^2$	1.406×10^{-5}	1.750×10^{-5}

Since the model is well fit to the data, the equation can be used to determine the slope of a line tangent to the curve at any point. This slope will be the change in delta linewidth for a given change in development time or exposure time, depending on the way the data are plotted (as in Figure 8 or as in Figure 9.) This is the sought-after process latitude, which is useful in determining the most forgiving operating point for photoresist processing. The results obtained pertain to the photoresist processing and are not related to the plasma etching step. For example, at an exposure time of 260 msec and a development time of 42 sec, a 0.1 μm change in linewidth is obtained for: a 12% decrease in exposure time, a 14% increase in exposure time, or a 24% increase or decrease in development time. Similar analysis can be performed over the entire variable ranges to obtain the optimum operating point.

The precision of a typical optical linewidth measurement system is 0.04 μm when measuring chrome on photomasks,[37] an optimum situation. The precision of a typical linewidth measurement system in an SEM is 5% of the linewidth being measured (0.1 μm for a 2.0 μm line). To determine the repeatability of the measurement system used in this study, one of the processed wafers was probed four times. The average and standard deviations for the change in linewidth were calculated for each separate probing of the wafer, and for the four measurements made on each die. These data are shown in Table 3. The average standard deviation within a wafer is 0.1 μm, and that of the four measurements on each die is 0.023 μm. The intrawafer variability is four times greater than the repeatability of the measurement system. This establishes intrawafer variations as the dominant factor in linewidth resolution for this work. The precision of this measurement system is better than that of the systems mentioned above.

Table 3: Repeatability of delta linewidth measurements (µm)

(nm = no measurement)

Die No.	Delta Linewidth (µm) 1	2	3	4	Mean	Standard Deviation
1	-0.82	-0.82	-0.82	-0.82	-0.820	0.000
2	-0.78	-0.78	-0.78	-0.78	-0.780	0.000
3	-0.79	-0.86	-0.84	-0.84	-0.833	0.030
4	-0.67	-0.67	-0.66	-0.66	-0.665	0.006
5	nm	nm	nm	nm	nm	
6	-0.75	-0.74	-0.71	-0.74	-0.735	0.017
7	-0.73	-0.72	-0.72	-0.73	-0.725	0.006
8	-0.71	-0.71	-0.71	-0.71	-0.710	0.000
9	-0.81	-0.78	-0.77	0.77	-0.783	0.019
10	-0.83	-0.78	-0.77	-0.77	-0.788	0.029
11	-0.63	-0.63	-0.62	-0.63	-0.628	0.005
12	-0.62	-0.63	-0.63	-0.64	-0.630	0.008
13	-0.79	-0.84	-0.85	-0.85	-0.833	0.029
14	-0.90	-0.76	-0.82	-0.82	-0.825	0.057
15	-0.65	-0.56	-0.59	-0.59	-0.598	0.038
16	-0.42	-0.48	-0.52	-0.47	-0.473	0.041
17	-0.74	-0.79	-0.80	-0.79	-0.780	0.027
18	-0.62	-0.60	-0.64	-0.64	-0.625	0.019
19	-0.70	-0.68	-0.70	-0.69	-0.693	0.010

Table 3 (cont)

Die No.	Delta Linewidth (μm) 1	2	3	4	Mean	Standard Deviation
20	-0.73	-0.62	-0.61	-0.60	-0.640	0.061
21	-0.74	-0.69	-0.69	-0.68	-0.700	0.027
22	-0.65	-0.69	-0.70	-0.70	-0.685	0.024
23	-0.62	-0.59	-0.58	-0.59	-0.595	0.017
24	nm	-0.62	-0.62	-0.62	-0.620	0.000
25	-0.84	nm	-0.88	-0.84	-0.853	0.023
Ave.	-0.72	-0.70	-0.71	-0.71	-0.74	0.023
S.D.	0.1	0.1	0.1	0.1	0.097	0.019

At the completion of the planned and randomized processing of the 25 wafers through the photolithography steps, five more wafers were processed at the center conditions (260 msec exposure time and 42 sec development time) to be used as controls. The 25 wafers were plasma etched in the randomized order, except that one of these controls was inserted at the beginning of the run, after five of the experimental wafers had been etched, after ten of the experimental wafers had been etched, and so on. The data from the five controls are shown in Table 4. All of the controls are within a standard deviation of each other, but the first three show a trend of increasing change in linewidth. This supports the possibility of a change in the etching as the etch chamber heats up.

Table 4: Delta linewidth (μm) for control wafers

Wafer No.	Average	Standard Deviation
28	-0.73	0.14
29	-0.77	0.14
30	-0.81	0.09
31	-0.79	0.11
32	-0.81	0.16

The results from the second experiment are shown in Table 5 and presented graphically in Figure 12. These results indicate that developer concentration is the dominant factor in controlling the photoresist linewidth. A 5% change in developer concentration results in a 0.5 μm change in linewidth. This means that the developer concentration must be controlled to within 1% to obtain 0.1 μm control over linewidth.

Table 5: Model coefficients for three-variable experiment

Term	Coefficient
Intercept	-5.24×10^{-1}
Dev. Conc.	-6.57×10^{-2}
Dev. Time	-2.27×10^{-2}
Exposure	-2.07×10^{-3}
$(\text{Dev. Time})^2$	-2.4×10^{-3}
$(\text{Dev. Conc.})^2$	-2.2×10^{-3}

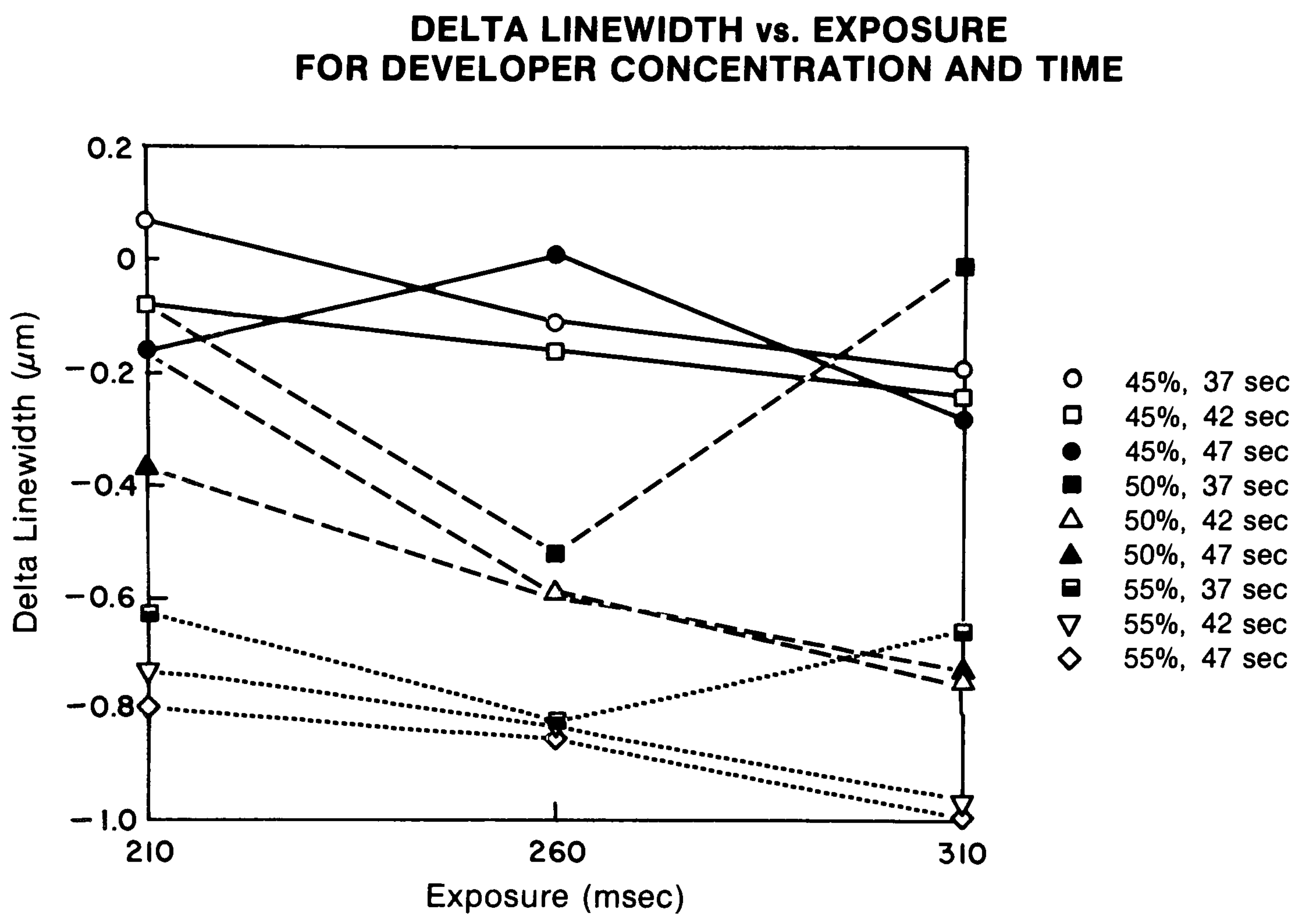


Figure 12: Delta linewidth vs exposure for development time and developer concentration.

In addition, one of the wafers from the second experiment was probed repeatedly for ten times. Data from this probing indicate a repeatability of 0.006 μm, which is even better than that obtained above.

VII. SUMMARY

Electrically testable linewidth structures were fabricated in doped polysilicon. Two typical, although abbreviated, photoresist characterization experiments were performed, and the results obtained provided the expected relationships between the chosen variables and the change in linewidth. The measured linewidth is the result of the entire patterning process: the photolithography and the etching step. From this information it is possible to obtain important process-latitude data.

The photoresist characterization process can be made easier by using DESRA or similar software to statistically design the experiments and to reduce the data and provide the relationships between the variables and the results. Automation of the data collection provides rapid turnaround compared to other data collection techniques. Lastly, even though full resist characterization requires much larger experiments and takes into consideration final resist thickness and profile, statistical experiment design and electrically testable linewidth structures can provide coherent and rapid progress toward this goal.

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APPENDIX

A. Processing Equipment:

1. Scrub/bake/coat/bake and develop/bake: Eaton Semiconductor Equipment Corp., Model LSI 45/60 (hot/cool plate ovens).

2. Exposure tool: TRE Semiconductor Equipment Corp., Model SLR 800, 10:1 wafer stepper.

3. Plasma equipment: Tegal Corp., Model 701 plasma etcher (polysilicon etch), Model 415 plasma etcher (resist strip.)

B. Photoresist and Developer:

1. KODAK Micro Positive Resist 820.

2. Experimental developer based on KODAK Micro Positive Developer 933.

C. Photoresist Processing:

1. Coat: dynamic dispense at 400 rpm, final spin speed 4800 rpm

2. Prebake: 45 sec at 130°C, 45 sec at 25°C

3. Postbake: 60 sec at 140°C, 60 sec at 25°C

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